30V 200mA Low Dropout LDO

1 Features

- Wide Input Voltage Range: up to 30V
- Output Current: 200mA
- Standard Fixed Output Voltage Options
  - 3.0V, 3.3V, 3.6V and 5.0V
- Low IQ: 1.5μA Typically
- <0.1μA Shutdown Current
- Dropout Voltage: 500mV at 100mA
- ±2% Output Voltage Accuracy
- Current Limit Protection
- Thermal Shutdown Protection
- Available Packages
  - SOT23-3, SOT23-5 and SOT89-3R

2 Applications

- Audio/Video Equipment
- Home Appliance
- Battery Powered Equipment

3 Description

The GD30LD2402 is a low dropout linear voltage regulator that features high input voltage, low dropout voltage, ultralow operating current. With quiescent current as low as 1.5μA, the GD30LD2402 is ideal for battery-powered equipment. The GD30LD2402 offers standard output voltages of 3.0V, 3.3V, 3.6V and 5.0V.

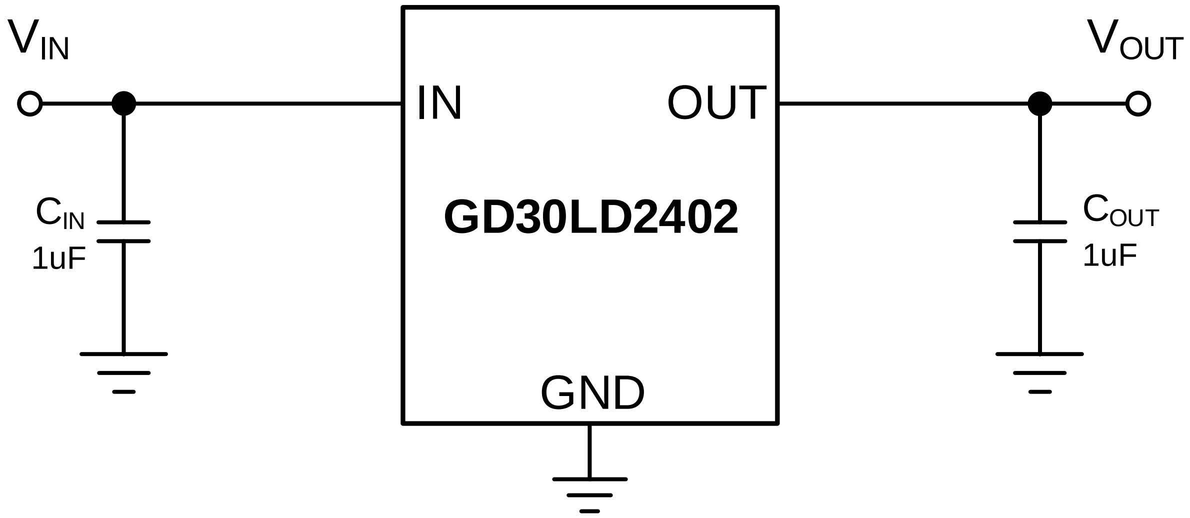
The GD30LD2402 is available in SOT23-3, SOT23-5 and SOT89-3R packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE(NOM)
GD30LD2402	SOT23-3	2.92mm x 1.60mm
	SOT23-5	2.92mm x 1.65mm
	SOT89-3R	4.50mm x 2.45mm

1. For all available packages, see the *Package Information* and *Ordering Information* at the end of data sheet.

Simplified Application Schematic



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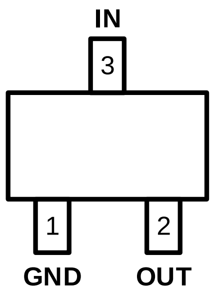
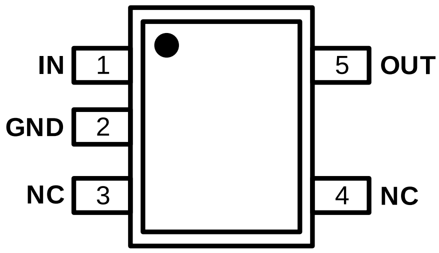
4 Device Overview

4.1 Pinout and Pin Assignment

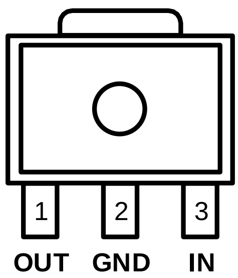
GD30LD2402BSTR-I
SOT23-3
(Top View)



GD30LD2402NSTR-S
SOT23-5
(Top View)



GD30LD2402BWTR-S
SOT89-3R
(Top View)



4.2 Pin Description

PIN NUMBER				PIN TYPE[1]	FUNCTION
NAME	SOT23-3	SOT23-5	SOT89-3R		
GND	1	2	2	G	Ground pin.
IN	3	1	3	P	Power supply input pin.
OUT	2	5	1	P	Output pin.
NC		3,4			No connection.

1. P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	IN	−0.3	36	V
V_{OUT}	OUT	−0.3	7	V
	VIN to VOUT	−0.3	31	V
PD	Power Dissipation, SOT23-3 @ T_A = 25°C		0.3	W
	Power Dissipation, SOT23-5 @ T_A = 25°C		0.3	W
	Power Dissipation, SOT89-3R @ T_A = 25°C		0.9	W
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−55	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	3		30	V
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±200	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-3	333	°C/W
		SOT23-5	333	°C/W
		SOT89-3R	111	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

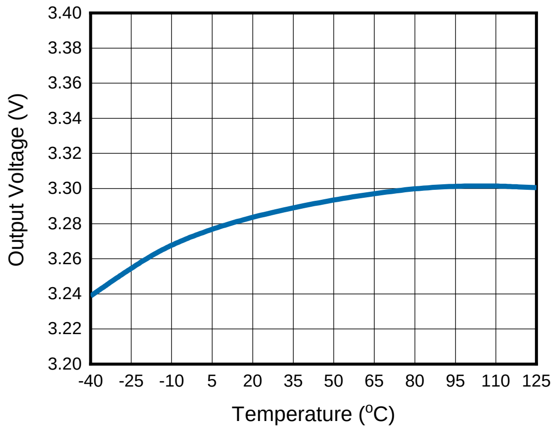
$V_{IN} = V_{OUT} + 2V$, $I_{OUT} = 10mA$, $C_{IN} = C_{OUT} = 1.0\mu F$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		3.0		30	V
V_{OUT}	Output voltage accuracy	$I_{OUT} = 10mA$	−2		+2	%
I_{OUT}	Maximum output current	$V_{IN} = V_{OUT} + 2V$		200		mA
I_Q	Quiescent current	$I_{OUT} = 0mA$		1.5	3	μA
V_{DO}	Dropout voltage[2]	$V_{OUT} = 5.0V$, $I_{OUT} = 100mA$		500		mV
		$V_{OUT} = 5.0V$, $I_{OUT} = 150mA$		750		mV
		$V_{OUT} = 3.3V$, $I_{OUT} = 100mA$		600		mV
		$V_{OUT} = 3.3V$, $I_{OUT} = 150mA$		850		mV
ΔV_{LINE}	Line regulation	$I_{OUT} = 1mA$		0.1		mV/V
ΔV_{LOAD}	Load regulation	$1mA \le I_{OUT} \le 150mA$		0.1		mV/V
I_{LIM}	Current limit	$V_{IN} = V_{OUT(NOM)} + 2V$		350		mA
T_{TSD}	Thermal shutdown temperature[1]			155		°C
T_{HYS}	Thermal shutdown hysteresis[1]			30		°C

1. Guaranteed by design and engineering sample characterization.
2. The dropout voltage is defined as V_{IN}- V_{OUT}, when V_{OUT} is 95% of the normal value of V_{OUT}.

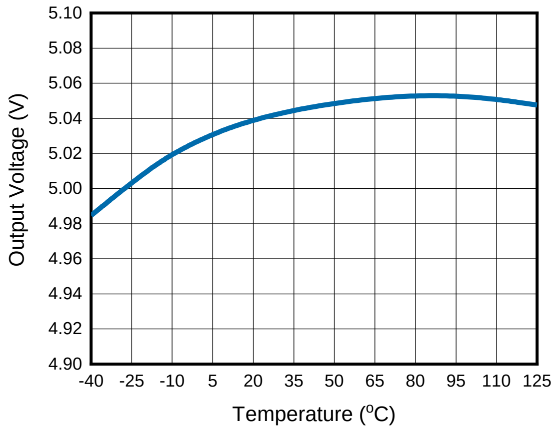
5.6 Typical Characteristics

C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise noted.



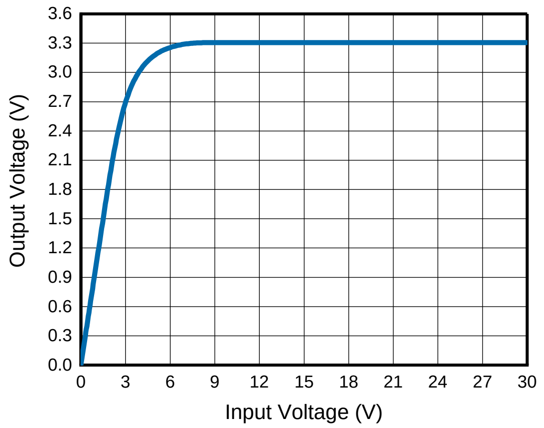
V_{IN}=4.3V, V_{OUT}=3.3V, I_{OUT} = 10mA

Figure 1. Output Voltage vs. Temperature



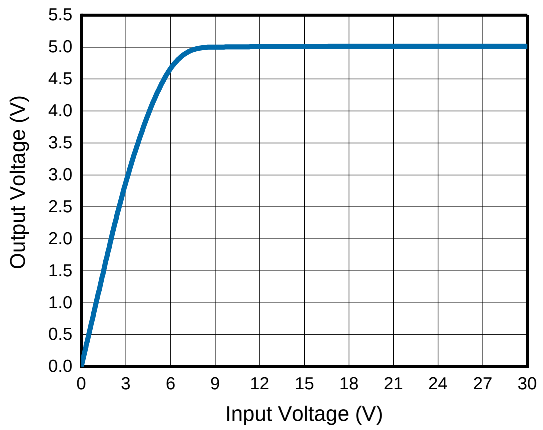
V_{IN}=6V, V_{OUT}=5V, I_{OUT} = 10mA

Figure 2. Output Voltage vs. Temperature



V_{OUT}=3.3V, I_{OUT} = 10mA

Figure 3. Output Voltage vs. Input Voltage

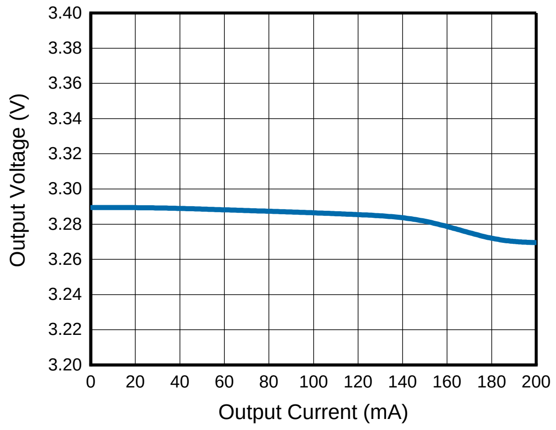


V_{OUT}=5V, I_{OUT} = 10mA

Figure 4. Output Voltage vs. Input Voltage

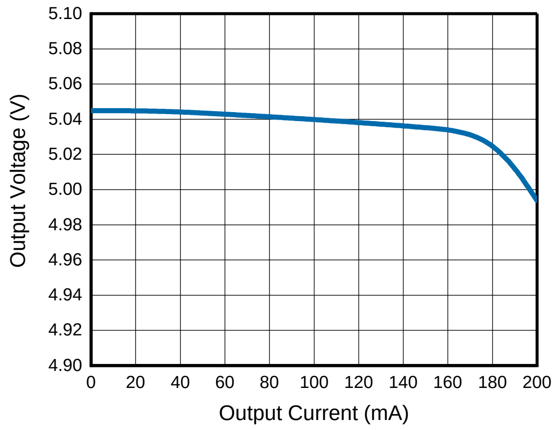
Typical Characteristics (continued)

$C_{IN} = C_{OUT} = 1.0\mu F$, $T_A = 25°C$, unless otherwise noted.



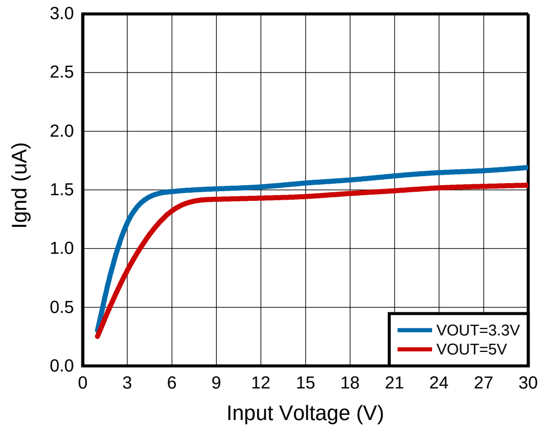
V_{IN}=4.3V, V_{OUT}=3.3V

Figure 5. Output Voltage vs. Output Current



V_{IN}=4.3V, V_{OUT}=3.3V

Figure 6. Output Voltage vs. Output Current



I_{OUT} = 0mA

Figure 7. Ground Current vs. Input Voltage

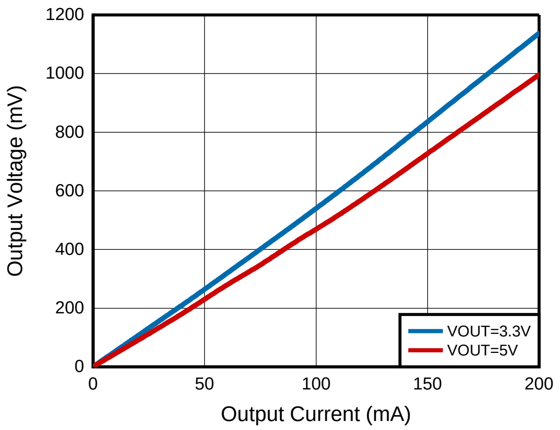


Figure 8. Dropout Voltage vs. Output Current

6 Functional Description

6.1 Block Diagram

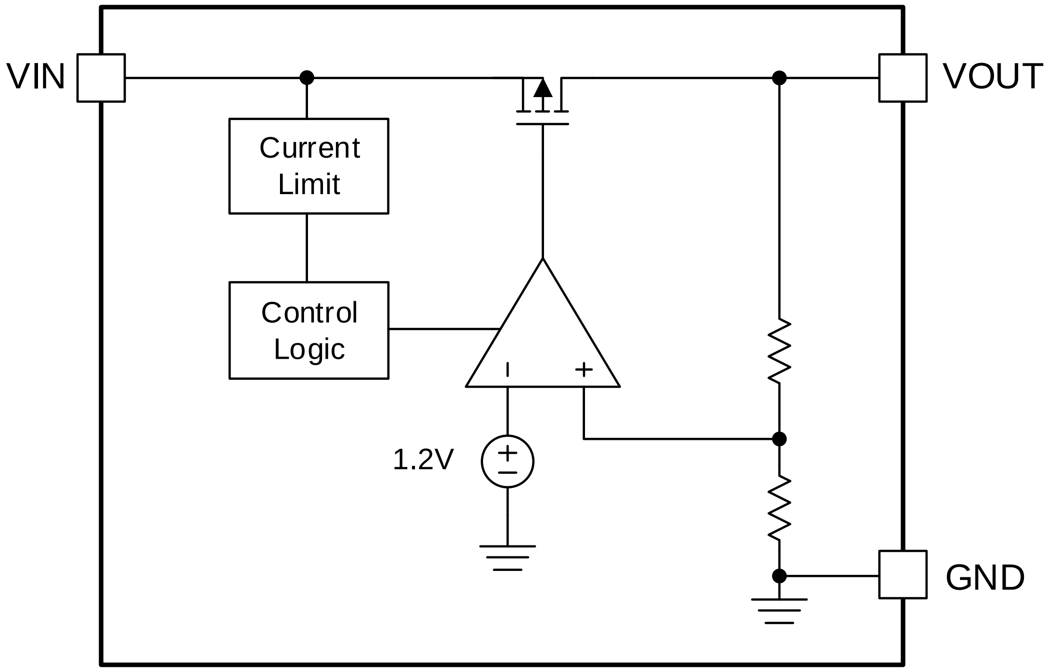


Figure 9. GD30LD2402 Functional Block Diagram

6.2 Operation

The external input and output capacitors of GD30LD2402 series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the device IN and GND pins. The GD30LD2402 series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Place the output capacitor close to the device OUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

6.2.1 Dropout Voltage

The GD30LD2402 series use a PMOS pass transistor to achieve low dropout. When (VIN – VOUT) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

6.2.2 Current Limit

The GD30LD2402 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 350mA (typical). The output can be shorted to ground indefinitely without damaging the part.

6.2.3 Thermal Shutdown

The over temperature protection function of GD30LD2402 series will turn off the P-MOSFET when the junction temperature exceeds 155°C (typical). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation.

7 Application Information

The GD30LD2402 is high voltage, low power consumption and low dropout LDO. Its output voltage is fixed, providing two versions with or without enable.

7.1 Typical Application Circuit

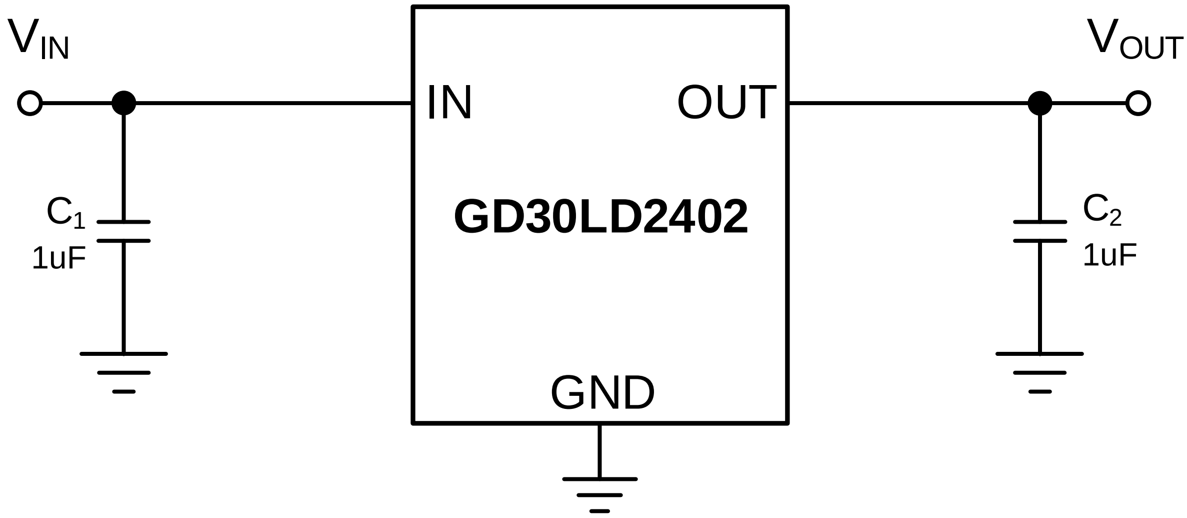


Figure 10. Reference Design Schematic

7.2 Detailed Design Description

7.2.1 Input Capacitor Selection

A 1μF or lager ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

7.2.2 Output Capacitor Selection

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1μF or lager, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

7.3 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

$V_{IN} \times V_{OUT}$ represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

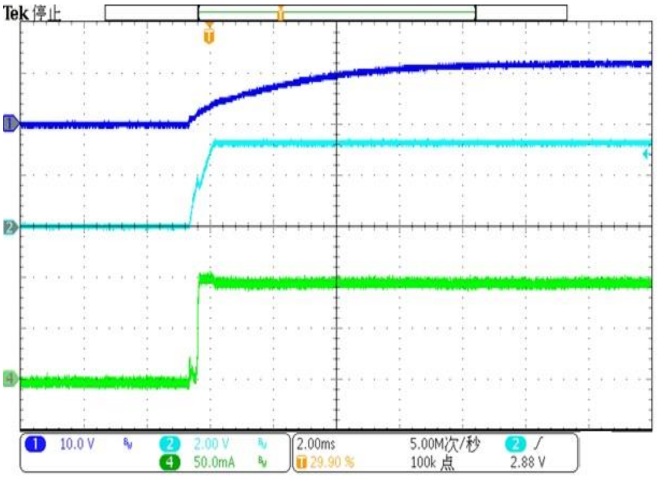
The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A). The maximum power dissipation can be calculated as below:

$$T_J = T_A + \theta_{JA} \times P_D \quad (2)$$

$$I_{OUT} = \frac{T_J - T_A}{\theta_{JA} \times (V_{IN} - V_{OUT})} \quad (3)$$

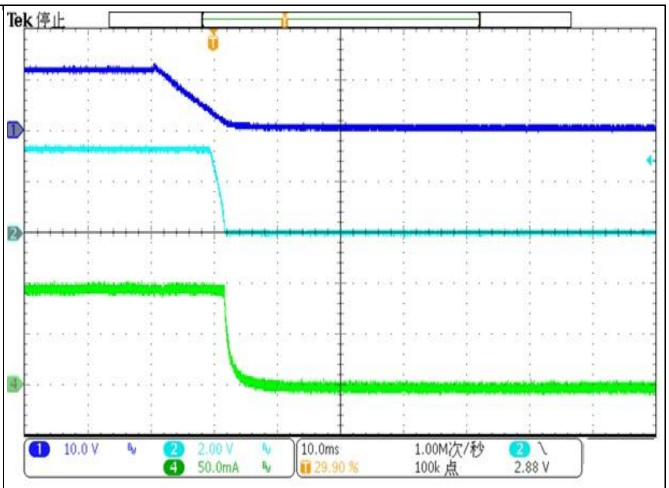
7.4 Typical Application Curves

$C_{IN} = C_{OUT} = 1\mu F$, $T_A = 25°C$, unless otherwise noted.



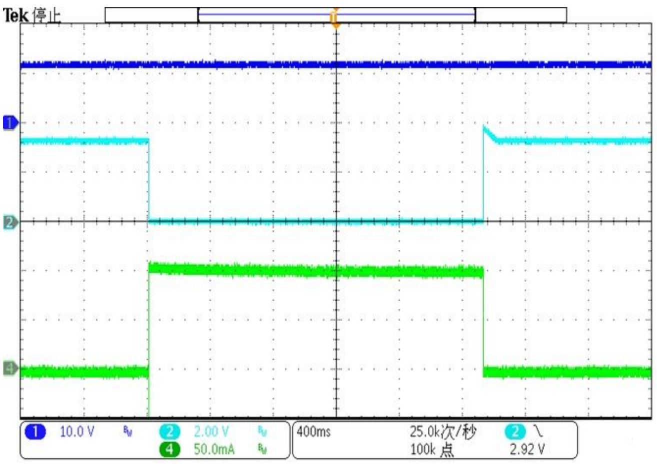
CH1=VIN, CH2=VOUT, CH3=IOUT

Figure 11. Power On With 200mA Load



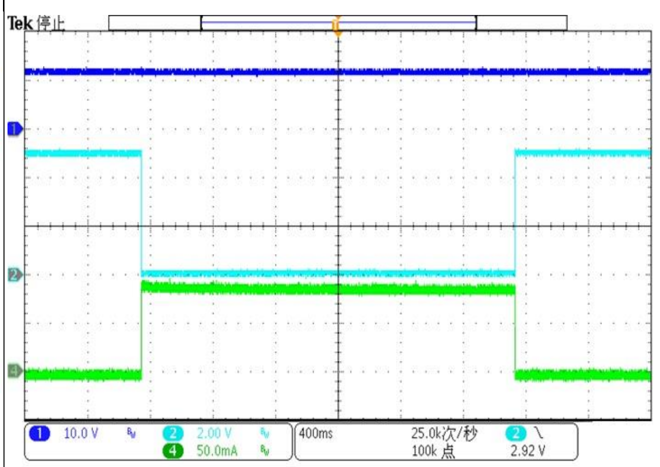
CH1=VIN, CH2=VOUT, CH3=IOUT

Figure 12. Power Off With 200mA Load



CH1=VIN, CH2=VOUT, CH3=IOUT

Figure 13. SCP Enter and Recovery



CH1=VIN, CH2=VOUT, CH3=IOUT

Figure 14. SCP Enter and Recovery

8 Layout Guidelines and Example

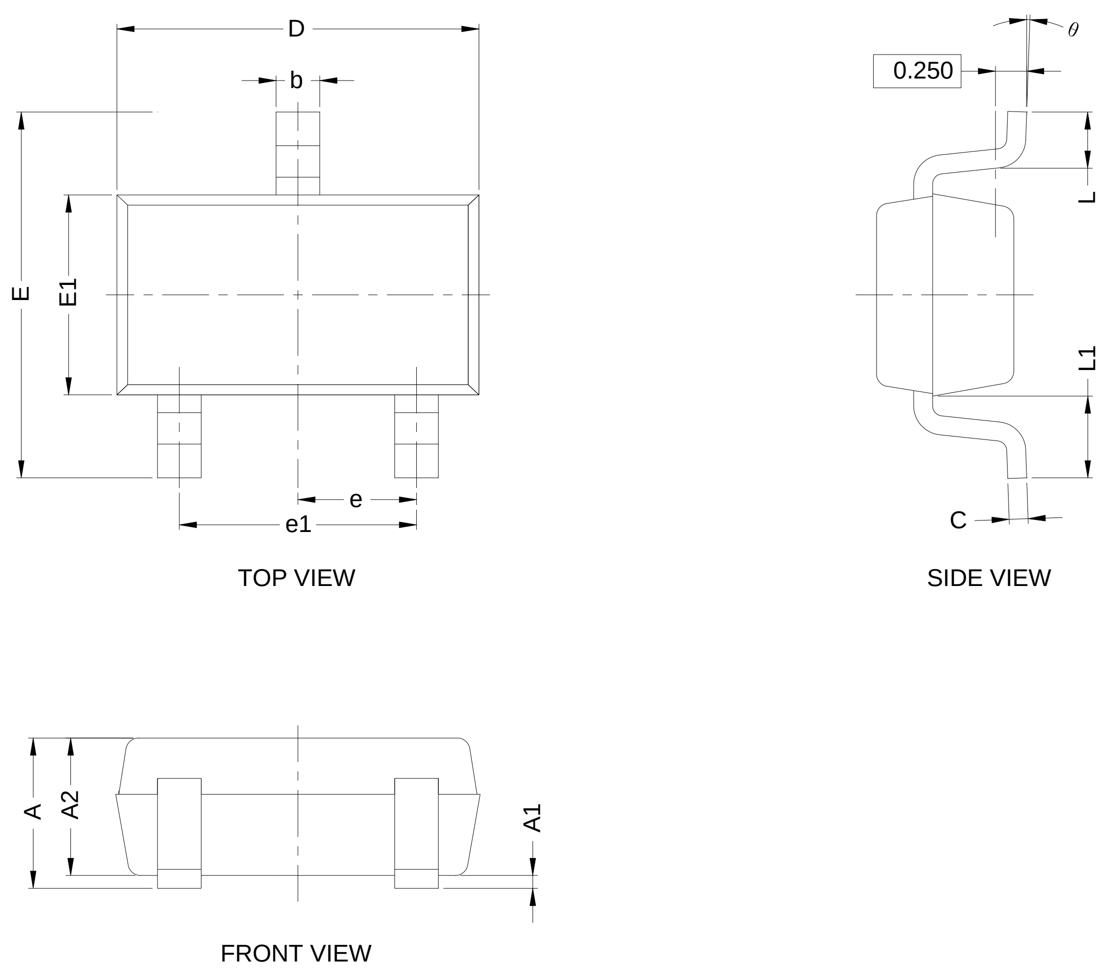
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the GD30LD2402 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

9 Package Information

9.1 Outline Dimensions

SOT23-3 Package Outline



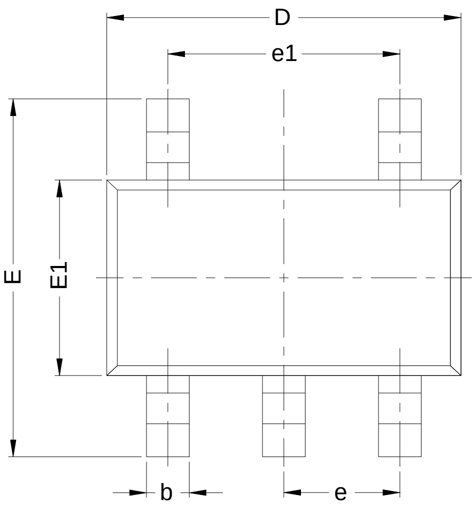
NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *SOT23-3 dimensions(mm)*.

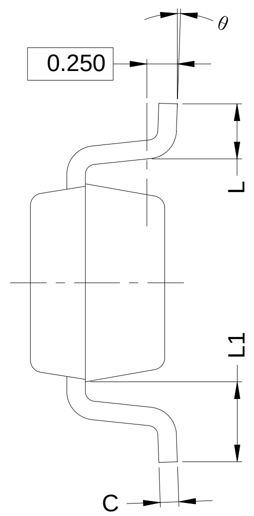
Table 1. SOT23-3 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.25
A1	0.00		0.10
A2	1.05	1.10	1.15
b	0.30		0.40
c	0.10		0.20
D	2.82	2.92	3.02
E	2.60	2.90	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.49	0.64	0.79
θ	0°		8°

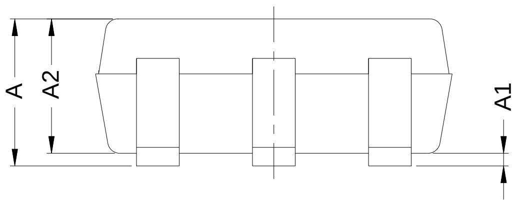
SOT23-5 Package Outline



TOP VIEW



SIDE VIEW



FRONT VIEW

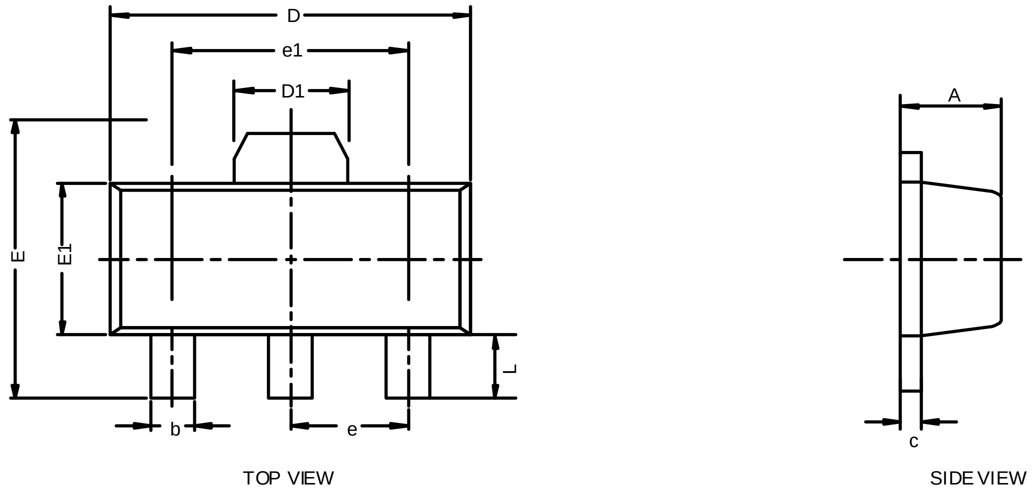
NOTES: (continued)

1. Refer to the Table 2 *SOT23-5 dimensions(mm)*.

Table 2. SOT23-5 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.25
A1	0.00		0.10
A2	1.05	1.10	1.15
b	0.35		0.50
c	0.08		0.20
D	2.82	2.92	3.02
E	2.60	2.90	3.00
E1	1.60		1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.49	0.64	0.79
θ	0°		8°

SOT89-3R Package Outline



NOTES: (continued)

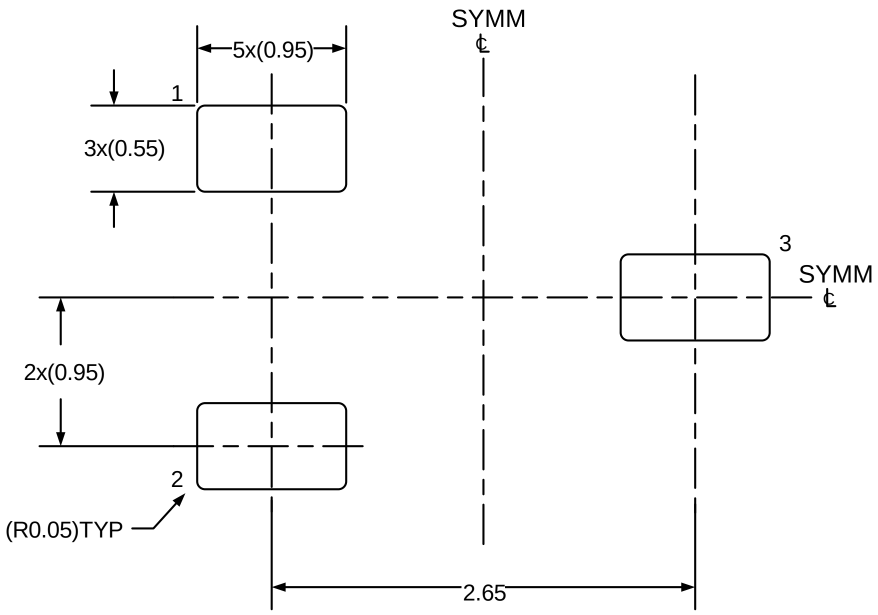
1. Refer to the Table 3 *SOT89-3R dimensions(mm)*.

Table 3. SOT89-3R dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	1.40		1.60
b	0.32		0.52
c	0.35		0.44
D	4.40		4.60
D1	1.55REF		
E	3.94		4.25
E1	2.30		2.60
e	1.50BSC		
e1	3.00BSC		
L	0.90		1.20

9.2 Recommended Land Pattern

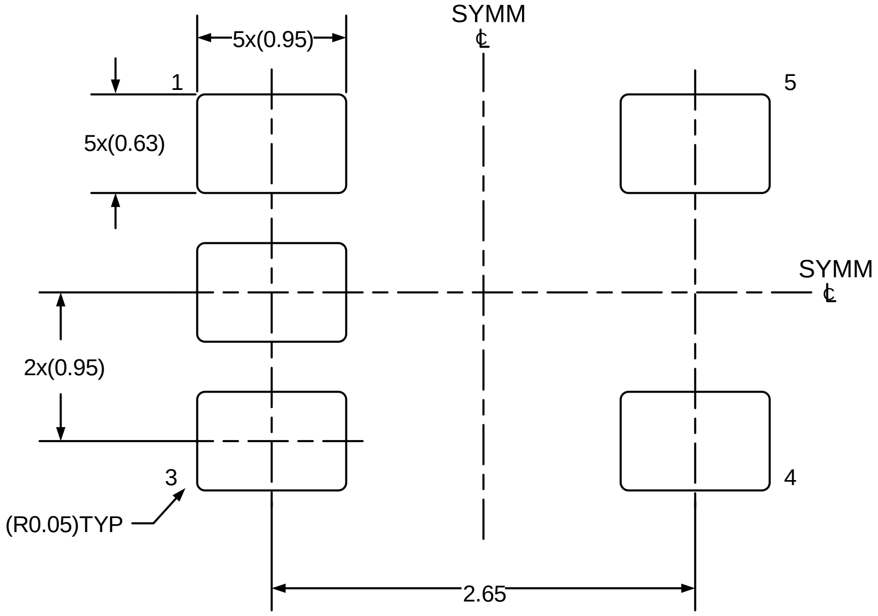
SOT23-3 Land Pattern Example



NOTES:

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

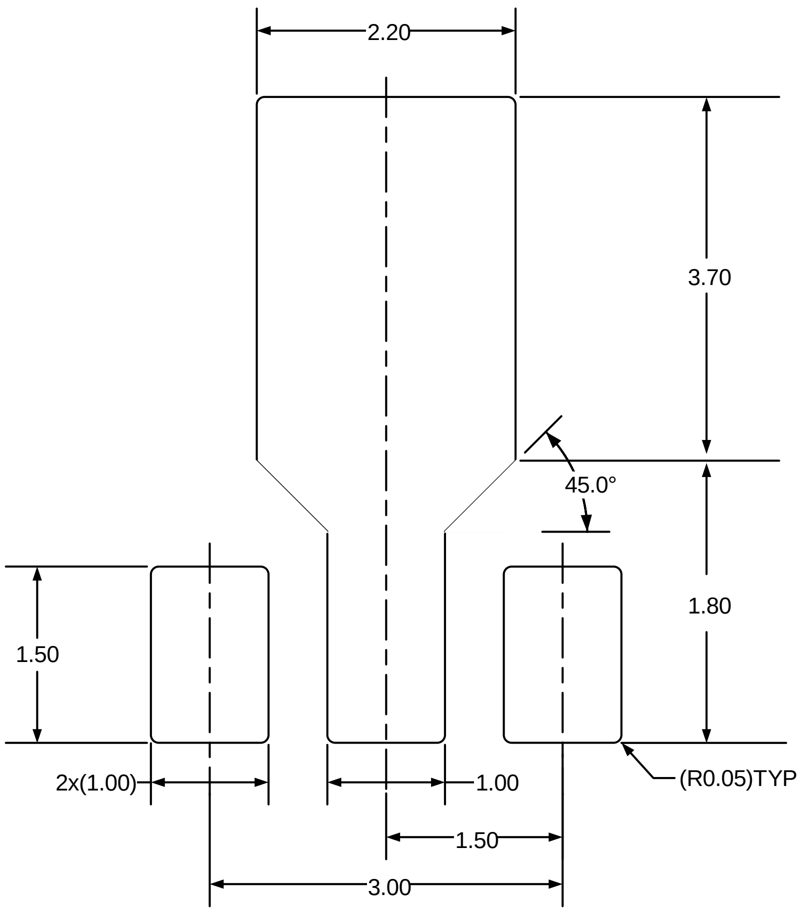
SOT23-5 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

SOT89-3R Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 15X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30LD2402BSTR-I30	SOT23-3	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402BSTR-I33	SOT23-3	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402BSTR-I36	SOT23-3	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402BSTR-I50	SOT23-3	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402NSTR-S30	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402NSTR-S33	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402NSTR-S36	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402NSTR-S50	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2402BWTR-S30	SOT89-3R	Green	Tape & Reel	1000	−40°C to +125°C
GD30LD2402BWTR-S33	SOT89-3R	Green	Tape & Reel	1000	−40°C to +125°C
GD30LD2402BWTR-S36	SOT89-3R	Green	Tape & Reel	1000	−40°C to +125°C
GD30LD2402BWTR-S50	SOT89-3R	Green	Tape & Reel	1000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023
1.1	Remove GD30LD2402BWTR-I package	2024

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